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A Survey Paper on Time-To-Digital Converter (TDC).

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ABSTRACT

In a profound CMOS submicron technology, the time resolution is always better than the voltage resolution. The system which detect the time information of a signal is called a TDC system.The basic task of TDC is to quantize the time interval between two signals with a resolution of some picoseconds. ADPLL is contributing great role inIndustrial, scientific and medical (ISM) band applications in wireless systems such as WLAN, WiMAX, Bluetooth and Zigbee.To design ADPLL for wireless communication, TDC are used for time interval measurement. All digital phase locked loop (ADPLL) is designed with digital components, which have high resistance to supply noise and temperature variation.

Keywords: Time-To-Digital Converter(TDC), All Digital Phase Locked Loop(ADPLL), Sense Amplifier Based Flip-Flop(SAFF), Gated Ring Oscillator(GRO), Switched Ring Oscillator(SRO), 2-dimension Vernier TDC(VTDC), 2-dimension Gated Vernier TDC (GVTDC), 3-dimension vernier ring TDC(3-D VRTDC).

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INTRODUCTION

Time-to-digital converter (TDC) is a sultry research topic[1]. Due to increasing usage of ADPLL, TDCs are developed more [2] [3]. TDC is similar to ADC, but while ADC converts analog information to digital, TDC converts in terms of time information to digital output. TDC's can be classified into two extremes: analog and digital as shown in fig:1. generally, analog TDC depend on current integration, while the digital TDC depend on some counting technique. Many TDC structures are introduced inbetween these two extremes.

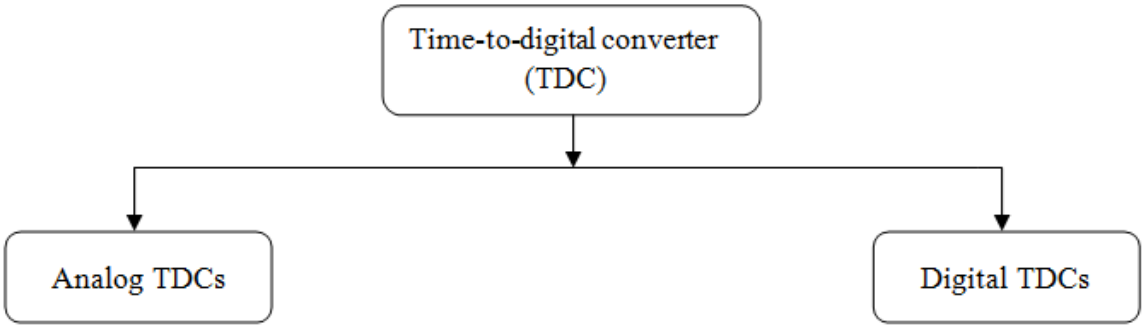

Fig 1: A classification of TDC

ANALOG TDC

Analog TDC is a traditional method, in the first place to change over the time interim to voltage. By using ADC voltage value is digitized. Pulse width can be created by habituating two events which is start and stop [4]. Using an analog integrator This pulse can be transformed to voltage by using analog integrator then the voltage can be bolstered to ADC. Dynamic range of analog TDC for N bit is

$$dynamicRange = 2^N \cdot T_{LSB} \qquad (1.1)$$

DIGITAL TDC

Analog TDC does not hold any scaling properties. Digital TDC does not have any analog conversion step and it is obviously ruled by digital circuitry. It specifically transform time interval into digital output [4]. High resolution can be accomplished. In digital TDC, time interval measurement can be done by using counter based TDC and digital delay line based TDC.

COUNTER BASED TDC

In counter based TDC, the time interim can be measured by counting the reference clock cycle. Fig.3 shows the estimation interim characterized by two signal (start & stop). It is thoroughly asynchronous to the clock signal. If the time interim is even smaller means high resolution can be accomplished. It can be done by more subdivision of clock signal. It should be in asynchronous manner as shown in fig 4. The device that plays out this subdivision is really called digital TDCs[4].

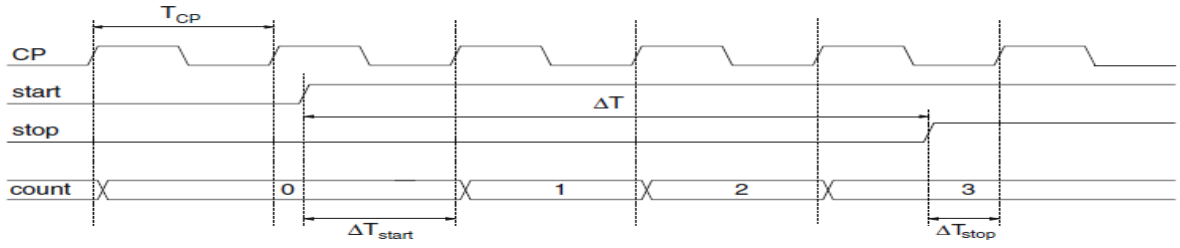

Fig 3: Time interim estimation of counter based TDC

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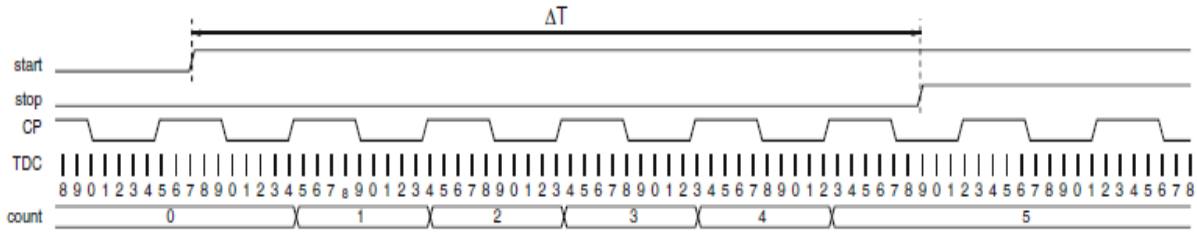

Fig 4: sub division of clock signal for high resolution

DELAY LINE BASED TDC

Fig.5 demonstrates the guideline of TDC in view of digital delay line. By using delay elements (inverter or buffer) the start signal is delayed and it is sampled by the entry of stop signal at the rising edge. The sampling process can be done by flip-flops. The delay line state can be freezes using flip flop when the stop signal occurs [4]. The yields of flip-flop will be 1'sand 0's.As a result, thermometer code will be generated.

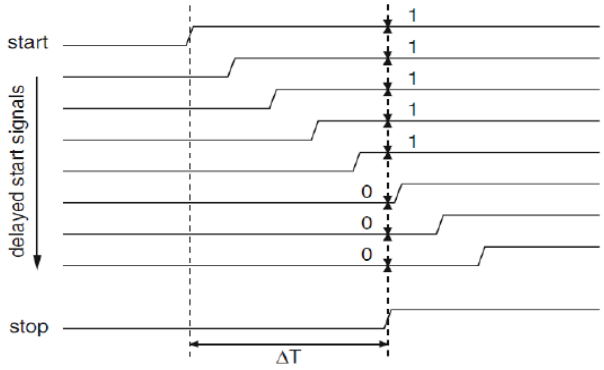

Fig 5: principle of delay line based TDC

MAJOR TYPES OF TDC

BUFFER DELAY LINE TDC

Start signal moves along the buffer chain and flip-flops are associated with the yields of buffers. The condition of delay line is examined by flip-flops when the stop signal arrives [5]. The D flipflop produces a thermometer code as a output demonstrating the separation amongst start and stop rising edges [6].One of the conspicuous focal points of this TDC is that it can be designed by totally digital. Consequently it is basic and conservative. Nonetheless, the resolution is moderately low since it is the delay of one buffer.

INVERTER DELAY LINE TDC

This TDC resolution will depend on delay of one inverter which is multiplied contrasted with buffer delay chain [6]. Completely symmetrical differential flipflops, for example, SAFF is utilized here[7] [8]. Start and complemented start signal moves along the two deferral chains. These difference informations are applied to the flipflops. In every alternative stage start and complemented input signal should be twisted. Here, resolution is constrained by technology. Layout implementation of this TDC is most challenging task.

VERNIER DELAY LINE TDC

Vernier TDC is equipped for measuring time interim with sub-gate resolution. It comprises start and stop signal delay lines. Both the signals are delayed. Start signal delay line is marginally bigger than the second line delay [9]. Amid the estimation, the begin signal proliferates along the main line and the stop signal

happens later. It appears like the stop signal follows start signal [10]. In every stage, it makes up for lost time by

TLSB= delay1- delay2 *(3.3.1)*

In this manner the resolution is subject to the distinction of two deferral stages rather than one buffer. It improves the resolution but area and power consumption. Conversion time also increased.

Table: 1 Comparison of Different TDC Architecture

REF. NO	ARCHITECTURE	DESCRIPTION	IMPROVEMENTS MADE
[14]	Two-dimensions Vernier TDC (2-D VTDC).	In this 2-D vernier plane all the conceivable differences between the tap will be considered. 2-D plane consists of comparator matrix and two delay axes.	• It reduces the length of delay chain leads to provide better efficiency. • More quantization levels can be produced
[15]	3-dimensional Vernier ring TDC (3-D VTDC).	3-D delay Space can be formed by adding more 2-D delay planes. It re-uses a comparator matrix and two delay rings.	• Efficiency and measurement time can be improved. Large DR can be achieved.
[16]	Vernier parallel delay-line TDC.	It combines vernier and parallel delay line TDC.	• It reduces mismatch, parasitic effects and conversion time. • It improves time resolution.
[17]	Vernier TDC using GRO in a 2-D pattern (2-D GVTDC).	It combines Vernier technique with a GRO. Classical vernier delay line is replaced by GRO.	• High raw resolution can be achieved. Latency time and Quantization noise can be reduced.
[18]	Switched-ring oscillator based TDC (SRO-TDC).	Operates at high oversampling ratios (OSRs).	• It is insusceptible to skew errors and leakage. Without using calibration high resolution can be achieved.
[19]	2-dimension Gated-Vernier TDC (2-D GVTDC) with digital GRO calibration.	Two 3-stage gated-ring oscillators (GRO)is used in x, y axes. It combines vernier and GRO concepts.	• It improves resolution. • Large latency time and quantization noise can be reduced.

GATED RING OSCILLATOR (GRO) TDC

For increasing TDC resolution effectively noise shaping technique should be used [11].GRO could accomplish expansive element range with little number of delay components. By protecting the oscillator state toward the end of the estimation interim Tin[k−1], the quantization blunder Tstop[k−1], from that estimation is additionally saved. Indeed, when the accompanying estimation of Tin [k−1] is started, the past quantization blunder is extended as Tstart[k] = Tstop[k−1] .Here, the result is the reduction of quantization noise in frequency domain. Here, 1st order noise shaping takes place [12]. In presence of large mismatch also high resolution can be achieved.

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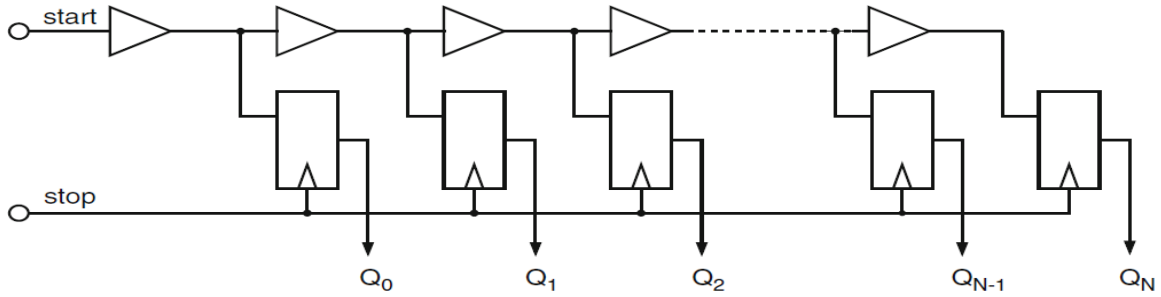

Fig 6: Buffer TDC

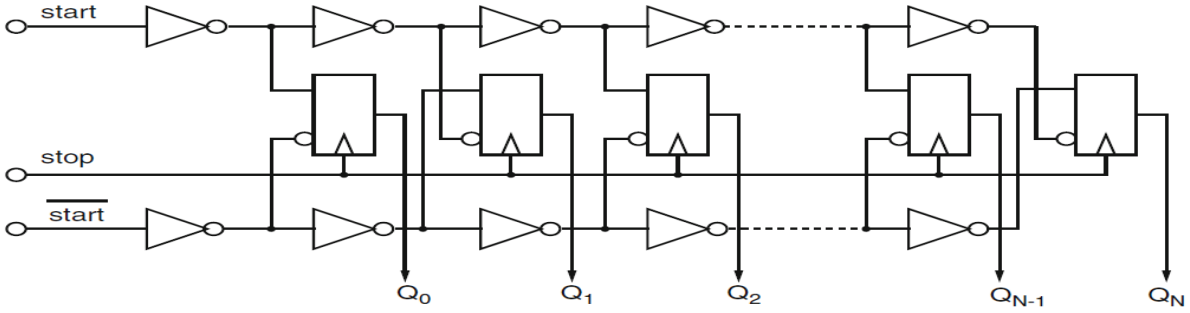

Fig 7: Inverter Delay Line TDC

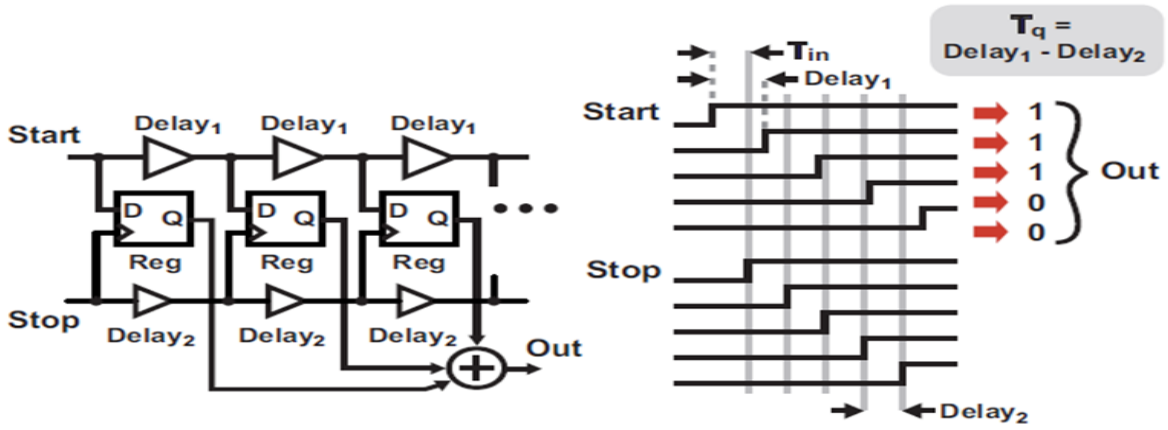

Fig 8: Vernier Delay Line TDC

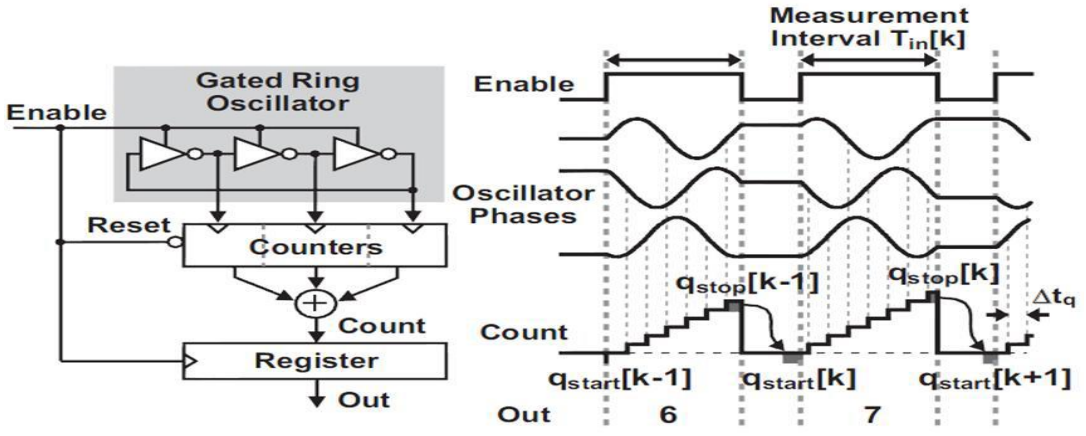

Fig 9: GRO TDC

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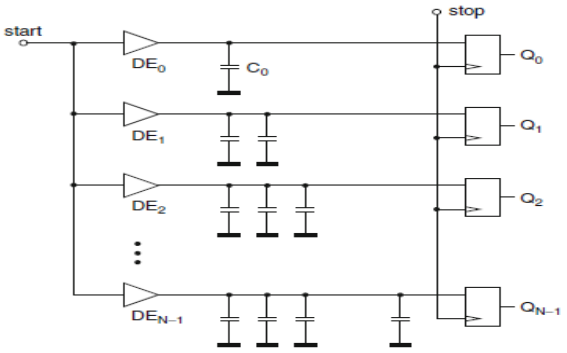

Fig 10: parallel scaled delay element TDC

PARALLEL SCALED DELAY ELEMENT TDC

Gates should be arranged in a parallel structure. Parallel produces TDC portrayed in Fig.10. The start signal connected to all delay components in parallel. The delay elements outputs are sampled at the same time when the stop signal rises [13]. Rather than proliferating the differential start signal, stop signal is deferred to keep away from differential discrepancy issue. The delay cells are associated with the stop signal are estimated for delays.

$$Td_i = Td0 + \Delta Td \cdot N \qquad (3.5.1)$$

The start and stop signal time difference is quantized. The resolution is T_{LSB} =Δtd. Output will be produced after the stop signal rises. Particularly for achieving a high DR, start and stop signal should be balanced. it is challenging one. It additionally implies that the layout is critical.

ADVANCED TDC ARCHITECTURE

TWO-DIMENSION VERNIER TDC (2-D VTDC)

The classical vernier TDC is arranged in two-dimension pattern forms a 2-D VRTDC. The number of delay element or length of delay chain can be reduced. In classical vernier structure uses more number of delay elements or stages. Classical vernier structure having demerit of low resolution, more power consumption, jitter noise and mismatches. Here, 2-D vernier TDC is proposed to overcome this problem[14]. Compared with classical vernier TDC, this proposed TDC provides high resolution. Here, power consumption and area is reduced. In a normal vernier plane, differential delay Δ can be computed between two delay chains. In the event that it is n stage implies nΔ differential delay can be acquired. Differential delay can be computed between the 1st stage of X and Y line . In 2-D plane, all conceivable differences between the taps can be obtained. Here, 25 quantization levels are obtained rather than 5.The time references are acknowledged with two delay lines. Using time comparator the digital conversion takes place.

3-D VERNIER RING TDC (3-D VRTDC)

Vernier ring TDC in a 3-dimension pattern is utilized. It significantly enhances the power consumption and measurement time. This TDC accomplishes fine resolution. At the same time, large detectable range also obtained .The number of delay element or length of delay chain can be reduced in 2D Vernier architecture. The same hardware can be utilized again and again in a ring configuration. So, this VRTDC enhances the detectable range without adjusting the resolution. The comparator matrix and two delay rings are utilized again and again in 3-D VRTDC[15]. This TDC incredibly enhances the power consumption, effectiveness and measurement time.

VERNIER PARALLEL DELAY LINE TDC

A new vernier parallel delay line TDC is utilized. For achieving fine resolution two parallel delay-lines are combined. The resolution of traditional delay-line TDC is characterized by the propagation delay of single delay element (inverter, buffer) utilized in delay chain. Different sub-gate delay line structures are developed for enhance the resolution. It includes parallel delay-line and Vernier-delay line based structures.The values of the single capacitors must be reduced for enhance the parallel TDC resolution. Parasitic effects of capacitor and mismatches are the constraints of parallel TDC if the capacitor is smaller. In this TDC architecture, it reduces the parasitic effects and mismatches for achieving finer time resolution[16]. For large n, this TDC conversion time is lower.

2-D VERNIER TDC USING GRO (2-D GVTDC)

This TDC combines Vernier technique with a GRO. Classical vernier delay line is replaced by GRO. A 2-D pattern GVTDC is used. All the conceivable differences between the taps can be obtained[17], as opposed to single stage line. The large latency time can be reduced. Using GRO minimum quantization noise of classical VTDC can be reduced. This TDC utilizes two GRO rather than two typical delayline. It enhances resolution. 2-D GVTDC combines the operation of GRO and Vernier TDC in 2-D design thus, it is advanced architecture the performance in terms of resolution, latency can be improved. In a classical vernier TDC, if the number of stage expanded means device mismatches will be expanded and an extensive latency is attained. To overcome this issue Vernier in view of ring oscillators TDC is utilized. Nonetheless, this Vernier-ring TDC has trade-off between TDC quantization noise and gain. GRO TDC utilizes noise shaping technique. Utilizing this procedure TDC resolution can be expanded completely and quantization noise can be minimized. Here, one GRO axis should be fast and other one should be slow.

SRO-TDC

This TDC utilizes switched ring oscillator with high OSRs. GRO TDC suffer from skew errors ,dead-zones and leakage. This TDC operates between two frequency states so it is insusceptible to leakage and skew errors and quantization noise can be reduced. Dead free zone operation is accomplished by repressing gating delay, charge distribution, leakage. By utilizing noise shaping and oversampling, high resolution can be accomplished without using calibration in SRO-TDC. In an open-circle way, noise shaping can be accomplished by switching of ring oscillator takes place between two frequencies. By separating the input carrier frequencies and sampling clock, SRO-TDC operates at high oversampling ratios[18].

2-D GVTDC WITH DIGITAL CALIBRATION

Two three-stage gated-ring-oscillators (GROs) used in 2-dimension (2-D) Vernier TDC. These two 3-stage GROsare used in the X and Y Vernier axes. Small quantization noise in classical VTDC is enhanced by GRO. Large latency time of the classical Vernier TDC is dramatically reduced. The output of N-stage GVTDC can be communicated as:

$$out_{TDC} = k \times X - (k-1) \times Y$$
$$k = \tau_1/\Delta,\ k-1 = \tau_2/\Delta,\ \Delta = \tau_1 - \tau_2$$

Where X indicates the tap of slow GRO delay and Y indicates the tap of fast GRO delay. GVTDC and 2-D GVTDC wish to characterize k in advance. Hypothetically, k in GVTDC is not really a number, but in a 2-D GVTDC k is an integer. In 2-D GVTDC, analog tuning is not a better immunity technique to noise. Digital calibration method is embraced in this TDC. It precisely characterizes k. It dramatically compensating for temperature and process variations. In the real chip, k is characterized by a digital calibration[19]. In the real execution, k is typically not a number and difficult to anticipate because of GRO delay variations. Its improved resolution and latency timeis highly used in DPLL applications.

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CONCLUSION

Different types of TDC and its block implementation have been presented. Some advanced TDC architecture and its comparison have been reported in detail. TDC is used in all digital PLLs, time of flight estimation and medical imaging application, signal capturing at high speed, data converters and demodulators. This paper also describes about two groups of TDCs which is analog and digital TDCs and its time interval measurement.

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